IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	R.A. Corley et al.
Case:	1-1
Serial No.:	10/630,961
Filing Date:	July 30, 2003
Group:	2609
Examiner:	Mon Cheri S. Davenport
Title:	Processor Configured for Efficient Processing of Single-Cell Protocol Data Units

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APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants (hereinafter "Appellants") hereby appeal the rejection dated June 5, 2008, of claims 1-14 of the above-identified application.

The fee previously paid with the prior Appeal Brief filed March 17, 2008 should be applied to the present Appeal Brief.

REAL PARTY IN INTEREST

The present application is assigned of record to Agere Systems Inc. On April 2, 2007, the assignee Agere Systems Inc. completed a merger with LSI Logic Corporation, with the resulting entity being named LSI Corporation. LSI Corporation is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on July 30, 2003 with claims 1-14, all of which remain pending. Claims 1, 13 and 14 are the independent claims.

Each of claims 1-14 stands rejected under 35 U.S.C. §103(a). Claims 1-14 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a processor comprising controller circuitry and first memory circuitry internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit. The processor is connectable to a second memory circuitry external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the processor recited in claim 1 are described in the specification at, for example, page 5, lines 1-19, with reference to FIG. 1. A processor (e.g., network processor 102) comprises controller circuitry (e.g., controller 120) and first memory circuitry (e.g., internal memory 104) internal to the processor. The controller circuitry is configurable to determine for a given protocol data unit received by the processor (e.g., from network 108) whether the given protocol data unit is a single-cell protocol data unit (see, e.g., page 5, lines 17-19, of the specification). The processor is connectable to a second memory circuitry (e.g., external memory 106) external to the processor. Information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a

single-cell protocol data unit (e.g., single-cell storage portion 122, described at page 5, lines 13-15, of the specification), and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., multi-cell linked list storage portion 124, described at page 5, lines 15-17, of the specification).

Independent claim 13 is directed to a method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to second memory circuitry external to the processor. The method comprises the steps of determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the method recited in claim 13 are described in the specification at, for example, page 7, line 6, to page 8, line 8, with reference to FIG. 3. A method (e.g., that shown in flow diagram 300) is suitable for use in a processor (e.g., 102 in FIG. 1) comprising controller circuitry (e.g., controller 120 in FIG. 1) and first memory circuitry (e.g., internal memory 104 in FIG. 1) internal to the processor. The processor is connectable to second memory circuitry (e.g., external memory 106 in FIG. 1) external to the processor. The method comprises the steps of determining for a given protocol data unit received by the processor (e.g., in step 302) whether the given protocol data unit is a single-cell protocol data unit (e.g., step 304); storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., step 306); and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., step 308).

Independent claim 14 is directed to a processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor. The processor is connectable to second memory circuitry external to the processor. The instructions when executed in the processor implement the steps

of determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Illustrative embodiments of the medium recited in claim 14 are described in the specification at, for example, page 6, lines 7-11, with reference to FIG. 1, and page 7, lines 21-22, with reference to FIG. 3. A processor-readable medium contains processor-executable instructions (e.g., software code, as recited in the specification at, for example, page 6, lines 7-11, with reference to FIG. 1, and page 7, lines 21-22, with reference to FIG. 3) for use in a processor (e.g., 102 in FIG. 1) comprising controller circuitry (e.g., controller 120 in FIG. 1) and first memory circuitry (e.g., internal memory 104 in FIG. 1) internal to the processor. The processor is connectable to second memory circuitry (e.g., external memory 106 in FIG. 1) external to the processor. The instructions when executed in the processor implement the steps of determining for a given protocol data unit received by the processor (e.g., step 302 in FIG. 3) whether the given protocol data unit is a single-cell protocol data unit (e.g., step 304 in FIG. 3); storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit (e.g., step 306 in FIG. 3); and storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit (e.g., step 308 in FIG. 3).

The claimed invention provides a number of significant advantages over conventional arrangements. In an illustrative embodiment, single-cell protocol data units are stored in an internal memory of the processor, thereby reducing the number of accesses to external memory. This results in improved processor performance and throughput. See also the specification at, for example, page 3, lines 9-13, and page 7, lines 6-13.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-14 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,278,834 (hereinafter "Mazzola") in view of U.S. Patent No. 5,499,348 (hereinafter "Araki").

ARGUMENT

Appellants respectfully traverse the §103(a) rejection on the ground that the Mazzola and Araki references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and further that no cogent motivation has been identified for combining the references or for modifying the reference teachings to reach the claimed invention.

In formulating the rejection of claim 1, the Examiner argues, with reference to FIG. 1 of Mazzola, that memory 14a and 14b are the recited first memory circuitry and memory 14c is the recited second memory circuitry. Even if one accepts these characterizations, Appellants respectfully submit that Mazzola still fails to teach or suggest the limitation of claim 1 wherein information characterizing a given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Rather than teaching the arrangement recited above, Mazzola instead teaches an arrangement wherein a single-cell protocol data unit is stored within a single memory buffer and a multiple-cell protocol data unit is stored in a linked list comprising multiple buffers. See, e.g., Mazzola at column 4, lines 3-25. However, whether a given protocol data unit is a single-cell protocol data unit stored within a single memory buffer or a multiple-cell protocol data unit stored in a linked list comprising multiple buffers, all memory buffers are allocated within buffer pool 14c (which, as discussed above, the Examiner characterizes as the recited second memory circuitry); see, e.g., Mazzola at column 3, lines 45-47; see also Mazzola at column 4, lines 3-11. Indeed, the Examiner concedes that buffer pool 14c stores single-cell protocol data units; see the present Office Action at page 3, first and second paragraphs (Memory 14c "is the buffer pool

from which memory buffer [sic] are allocated. . . . [T]he buffer contains a protocol data unit big enough to be transmitted as [sic] single data unit.")

Accordingly, Mazzola fails to teach or suggest the claimed arrangements in which information characterizing a given protocol data unit received by a processor is stored in first memory circuitry internal to the processor if the received protocol data unit is a single-cell protocol data unit, and is stored in second memory circuitry external to the processor if the received protocol data unit is not a single-cell protocol data unit.

In the present Office Action at page 2, last paragraph, the Examiner argues, with reference to FIG. 1 of Mazzola, that memory 14a and 14b are the recited first memory circuitry internal to the processor because memory 14a and memory 14b are used for internal functions of processor 12. Appellants respectfully disagree. As noted above, claim 1 is directed to a processor comprising first memory circuitry internal to the processor. Appellants respectfully submit that claim 1 therefore requires that the processor itself contain the recited first memory circuitry. See also the illustrative embodiments of the claimed arrangements described in the present specification at, for example, page 4, lines 22-28 (describing "an internal memory of the network processor" and "a memory external to the network processor"); page 5, lines 12-19 (with reference to FIG. 1); and page 8, lines 10-14 (with reference to FIG. 4).

Appellants respectfully note that memory 14a and memory 14b each refer to areas within memory 14. See, for example, Mazzola at FIG. 1 and at column 3, lines 39-48. Mazzola expressly indicates that memory 14, and hence 14a and 14b, is not contained within processor 12. See, for example, Mazzola at FIG. 1 and at column 3, lines 13-15 ("Each end system node 10 has a processor 12 in communication with a memory 14").

In the present Office Action at page 3, fourth paragraph, the Examiner asserts that Mazzola fails to disclose an arrangement wherein the first memory is internal to the processor, which appears to be inconsistent with the Examiner's argument found in the present Office Action at page 2, last paragraph. The Examiner relies on Araki's disclosure of an instruction memory internal to a processor to supplement the teachings of Mazzola so as to reach the limitations of claim 1.

Appellants respectfully submit that Mazzola teaches a conventional arrangement similar to that described in the present specification at page 2, lines 1-13, in which a memory external to a processor is used to store all protocol data units, regardless of whether or not such protocol data units are single-cell units. Appellants respectfully submit that nowhere does Araki contain any teaching or suggestion which would supplement Mazzola so as to reach the limitations of claim 1 wherein information characterizing a given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit, and information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

Indeed, Araki contains no teachings or suggestions directed to storage of protocol data units in a memory internal to a processor, or indeed any storage or processing of protocol data units, much less the specific arrangement recited in claim 1. Rather, Araki at column 3, lines 52-66, with reference to FIG. 1, discloses that a digital processor 101 including instruction memory 102 which stores instruction codes.

Moreover, even if Mazzola could somehow be combined with Araki so as to reach the limitations of claim 1, Appellants respectfully submit that Araki is not analogous prior art and therefore cannot form the basis for a rejection under 35 U.S.C. §103. See, e.g., *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992) ("In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned."); *In re Clay*, 966 F.2d 656, 659, 23 USPQ2d 1058, 1060-61 (Fed. Cir. 1992) ("A reference is reasonably pertinent if, even though it may be in a different field from that of the inventor's endeavor, it is one which, because of the matter with which it deals, logically would have commended itself to an inventor's attention in considering his problem.").

Appellants respectfully submit that Araki, which is completely unrelated to storage or processing of protocol data units, is not in the field of applicant's endeavor. See *Wang Lab. v. Toshiba Corp.*, 993 F.2d 858, 864 (Fed. Cir. 1993) (holding that "art is not in the same field of endeavor as the claimed subject matter merely because it relates to memories."). Indeed, there appears to be no reason why Araki logically would have commended itself to an inventor's

attention in considering his problem, much less have been an obvious candidate for combination with Mazzola.

Furthermore, even if it were possible to combine Mazzola and Araki so as to meet the limitations of claim 1, the Examiner has failed to provide a legally sufficient explanation for why one skilled in the relevant art, having no knowledge of the claimed invention, would have done so. See, e.g., *In re Kotzab*, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also *KSR v. Teleflex*, 127 S.Ct. 1727, 1741, 82 USPQ2d 1385, 1396 (U.S., Apr. 30, 2007) ("[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known."); *Id.* (The analysis of "whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue . . . . should be made explicit.")

Rather, Appellants respectfully submit the Examiner's assertion that it would have been obvious to combine Mazzola with Araki because Araki "improves the throughput of the total processing" appears to be precisely the type of conclusory statement ruled legally insufficient by the both Supreme Court and the Federal Circuit. See *KSR*, 127 S.Ct. at 1741, quoting *In re Kahn*, 441 F. 3d 977, 988 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.").

Moreover, even if one were to assume for purposes of argument that the Examiner has established a proper *prima facie* case of obviousness, Appellants respectfully submit that there is sufficient evidence of nonobviousness so as to rebut any such *prima facie* case. For example, the fact that others have used a less advantageous technique, rather than combining the teachings disclosed in the cited references, suggests both a long-felt need and failure of others.

Appellants note that Mazzola was filed in 1992 and issued in 1994, and that Araki was issued in 1996, based on a foreign application filed in 1990. Appellants respectfully submit that the failure of other researchers in Appellants' field of endeavor to render the allegedly obvious invention disclosed in the present application, despite the considerable advantages that

Appellants have determined result from such an arrangement, during the long period during which both references were publicly available and presumably well known to those skilled in the art constitutes objective evidence of non-obviousness and only further lends support for the patentability of the present invention.

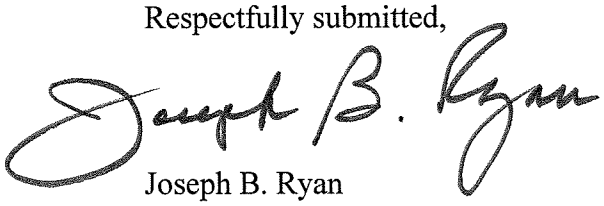
In view of the above, Appellants respectfully submit that the combination of Mazzola and Araki fails to render claim 1 obvious.

Independent claims 13 and 14 include limitations similar to those of claim 1, and are believed allowable for reasons similar to those described above with reference to claim 1.

Dependent claims 2-12 are believed allowable for at least the reasons identified above with regard to claim 1.

In view of the above, Appellants believe that claims 1-14 are in condition for allowance, and respectfully request the reversal of the §103(a) rejection.

Respectfully submitted,



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CLAIMS APPENDIX

1. A processor comprising:

controller circuitry configurable to determine for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit; and

first memory circuitry internal to the processor;

the processor being connectable to second memory circuitry external to the processor;

wherein information characterizing the given protocol data unit is stored in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

wherein information characterizing the given protocol data unit is stored in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

2. The processor of claim 1 wherein the protocol data unit comprises a packet.

3. The processor of claim 1 wherein the single-cell protocol data unit comprises a protocol data unit having a size less than or substantially equal to that of a cell-based processing unit of a switch fabric associated with the processor.

4. The processor of claim 1 wherein the information characterizing the given protocol data unit comprises at least one block descriptor.

5. The processor of claim 4 wherein the block descriptor is associated with a particular data block of the given protocol data unit.

6. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the first memory circuitry without requiring utilization of a linked list data structure.

7. The processor of claim 1 wherein the information characterizing the given protocol data unit is stored in the second memory circuitry utilizing a linked list data structure.

8. The processor of claim 1 wherein the processor is configured to provide an interface for communication of the protocol data unit between a network and a switch fabric.

9. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a queuing and dispatch buffer memory of the processor.

10. The processor of claim 1 wherein at least one of the first memory circuitry and the second memory circuitry further comprises a protocol data unit buffer memory of the processor.

11. The processor of claim 1 wherein the processor comprises a network processor.

12. The processor of claim 1 wherein the processor is configured as an integrated circuit.

13. A method for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the method comprising the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

14. A processor-readable medium containing processor-executable instructions for use in a processor comprising controller circuitry and first memory circuitry internal to the processor, the processor being connectable to second memory circuitry external to the processor, the instructions when executed in the processor implementing the steps of:

determining for a given protocol data unit received by the processor whether the given protocol data unit is a single-cell protocol data unit;

storing information characterizing the given protocol data unit in the first memory circuitry if the given protocol data unit is a single-cell protocol data unit; and

storing information characterizing the given protocol data unit in the second memory circuitry if the given protocol data unit is not a single-cell protocol data unit.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None